Energy Dissipation of MMC-HVDC based Onshore Wind Power Integration System with FB-DBS and DCCB

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Abstract: With the development of HVDC, MMC is seeking its application in onshore wind power integration. AC and DC faults are important issues for the wind power integration system, during which the wind generation system continuously provides wind power and the surplus power may cause overvoltage to sub-modules of MMC. This paper focuses on the energy dissipation during AC and DC faults for the overhead-line MMC-HVDC system integrating large scale wind power. A two-terminal MMC-HVDC system with permanent magnet synchronous generator (PMSG) based wind farm is studied. Hybrid DC current breakers (DCCBs) are employed to interrupt DC fault current and the method based on measuring the rate of change of DC line voltage is adopted to trip DCCBs. Also a full-bridge sub-module based dynamic braking system is implemented at the DC link to absorb the surplus wind power in case of AC or DC faults in the HVDC grid. To ride-through AC and DC faults without blocking IGBTs, the control of hybrid DCCB and the system fault ride-through (FRT) strategies are properly designed. PSCAD/EMTDC simulations are shown to demonstrate theoretical analysis.

1. Introduction

Driven by the transition from conventional fossil energy towards a renewable and sustainable energy system, the wind power utilization has been acknowledged as one of the most promising approaches [1]-[3]. Till 2018, 591 GW wind power has been installed world widely including both onshore and offshore wind power [4]. Due to the intermittence and fluctuation characteristics of wind power, integration using the modular multilevel converter (MMC) based HVDC is recognized as an efficient scheme [5][6]. There are many commissioned MMC-HVDC based offshore wind farm integration projects, especially in Europe, e.g. the *BorWin*, *DolWin*, *Helwin* and *SylWin* projects[7]-[9].

However, the offshore wind power integration only possesses about 9% of the global annual market [4]. For China, Brazil and some other countries, the onshore wind power integration accounts for a larger proportion. Different from the offshore wind integration system using submarine DC cables to transmit power, to integrate large-scale inland wind farms from remote areas to the load centre, the overhead lines based transmission is preferred.

For the MMC-HVDC based onshore wind power integration system, once an AC fault happens at the grid side, the active power generated by the wind plants cannot be transmitted to the receiving grids, leading to the increase of DC link voltage[10]. The overvoltage will cause the breakdown of power electronic devices inside the converters. To reduce the injected wind power, coordination control strategies can be designed for the MMC at wind farm side. Reference [11] proposes a cascaded droop control to adaptively reduce the wind power during onshore AC faults. The cascaded droop control adopts the v_{dc}-v_{ac} droop control for the wind farm side MMC (WFMMC) and the v_{ac}-P droop control for the wind farms, which speeds up the response time of the system control to AC faults, but all the MMCs are influenced during the fault. Reference [12] adopts a droop controller based on DC voltage variation to reduce the power injected into the multi-terminal DC (MTDC) grid by reducing the AC voltage at the integrating point. Although this measure can reduce the power injected into the HVDC system, the surplus wind power still needs to be dissipated. In direct drive permanent magnet synchronous generator (PMSG) based wind farm, using DC choppers to dissipate the surplus power results in increase of footprint and volume of wind power generators [13][14]. Thus, to ensure the safety of converters and DC grids, additional dynamic braking systems (DBS) as disclosed in [15] are proposed to absorb the surplus wind power.

Moreover, the overhead lines are prone to DC faults. To tackle with the DC faults, high power DC circuit breakers (DCCBs) can be adopted to interrupt the DC fault current. Then, the output wind power will be injected into the sub-modules of WFMMC and the metal oxide varistor (MOV) branch of DCCBs, endangering the safety operation of converters and electronic devices [16]. On the other hand, the surplus wind energy injected into the MOV branch imposes high requirements for the arrester, which leads to high construction cost of DCCBs [17].

To address the above challenges, several kinds of DBS are proposed in [18][19] to dissipate the wind power during faults. Prior researches have been carried out on the installation location of DBS, which is at the onshore side to enable un-interrupted operation of the system during onshore AC faults [18][19]. Another method is to install DBS at the AC side of WFMMC, but the three-phase configuration requires much space. Installing DBS at the DC side of WFMMC, closer to the converter station than the DC reactor, such as the DC chopper configuration is a better choice, which has the simplest topology and least number of power semiconductors, but generates high *di/dt* and *dv/dt* during operation and is unable to match high voltage level. The DBS based on distributed resistors has low *di/dt* and *dv/dt*, but requires water cooling system [15]. In addition,

conventional energy dissipation devices adopting a series diode connected resistor scheme have high stress requirements on the switching device.

This paper proposes a full-bridge based dynamic braking system (FB-DBS) cooperating with DCCBs to realize fault ride-through and energy dissipation of the MMC-HVDC based onshore wind power integration system. During DC faults, DCCBs are tripped in a few milliseconds and the FB-DBS will be put into operation to dissipate the surplus power generated by the wind farm. During AC faults, the surplus power is absorbed by FB-DBS.

This paper is organized as follows. Section II introduces the topology of the study system briefly. Section III analyses the operating principle, control strategy and parameter design of FB-DBS. Section IV proposes the control of hybrid DCCB and the fault ride through (FRT) strategies during AC and DC faults. In section V, the simulation results demonstrate the validity of the fault ride through scheme. Conclusions are drawn in section VI.

2. System Configuration

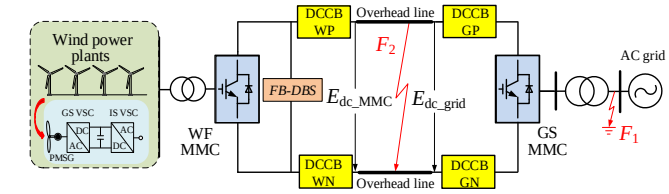


Fig.*1* shows the topology of a typical MMC-HVDC based wind power integration system. The wind farm plant is consisted of several PMSGs. Each PMSG is connected to a full-power converter, which is consisted of a generator side VSC (GS VSC) and an integration side VSC (IS VSC). The wind power is transmitted to the power grid through 300 kilometres overhead lines. GSMMC and WFMMC adopt the half bridge MMC topology. In normal operation, the WFMMC is used to control AC voltage of the integration point and the GSMMC is used to control the DC voltage of HVDC link.

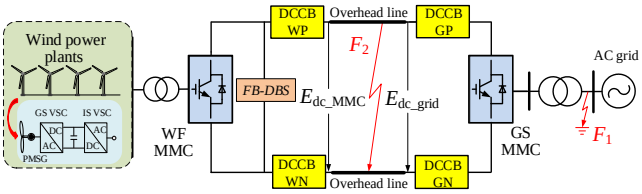


Fig.1. *PMSG based inland WPP using MMC-HVDC integration*

To ride though DC faults, four high power DCCBs are installed at the terminals of overhead lines. These DCCBs adopt the hybrid DCCB topology disclosed in [17]. It is composed of a main branch, a commutation branch and an absorption branch [20]. The basic structure of each hybrid DCCB is shown in in Fig.2.

To dissipate the surplus energy during AC and DC faults, an FB-DBS is proposed and installed at the DC terminal of WFMMC.

In normal operation, the ultra-fast-disconnector (UFD) of hybrid DCCB is closed and the DC current flows through the load commutation switches (LCS) to GSMMC. The output voltage of the cascaded FB sub-module (FBSM) in FB-DBS is maintained at the rated DC voltage, preventing DC current from flowing to the energy dissipation resistor.

When a DC fault is detected, the four DCCBs will be instantaneously tripped (within 3ms), forcing DC current to the commutation branch by opening the UFD switch. And then, the output voltage of cascaded FBSM in DBS is controlled to decrease to drive the energy dissipation resistor absorbing power. Once the fault is cleared, DCCBs will be reclosed and the DBS will automatically exit operating. Thus, the system recovers to normal operation.

Under AC faults at the grid side, DCCBs will not operate, and only the DBS will be utilized to dissipate the surplus wind power. The control principle of DBS is similar to that during DC fault. Once the AC fault is eliminated, the DC voltage of the overhead line recovers to normal operation and the DBS automatically turns off.

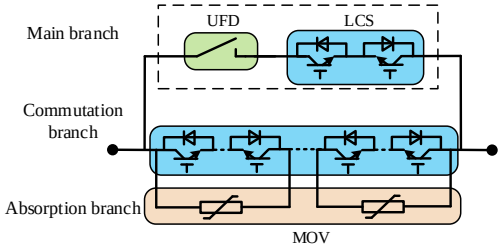


Fig.2. *Basic structure of hybrid DC circuit breaker*

3. Structure and Control Design of FB-DBS

3.1. The configuration of FB-DBS

The configuration of FB-DBS is shown in Fig.3. It is composed by serial connection of cascaded FBSMs, a lumped resistor r and a lumped capacitance C_{fl}. V_{cf} is the voltage produced by full-bridge sub-modules, I_{DBS} is the current flowing through the arm and r, V_{CMi} is the voltage of SM_i capacitor which can be set as zero, $+V_{Ci}$ or $-V_{Ci}$ depending on the operating status of FBSM. The cascaded FBSM is used to control the terminal voltage and instantaneous power of the energy dissipation resistor by adjusting its output voltage to compensate part of the DC line voltage. The lumped resistor r is used to absorb surplus power during faults. Besides, the lumped capacitance C_{fl} is used to eliminate the harmonics generated by cascaded FBSM dynamic switching.

During the operating process, the cascaded FBSM controls its output voltage to decline through a preset modulation wave, so that its *di/dt* and *dv/dt* can be restricted.

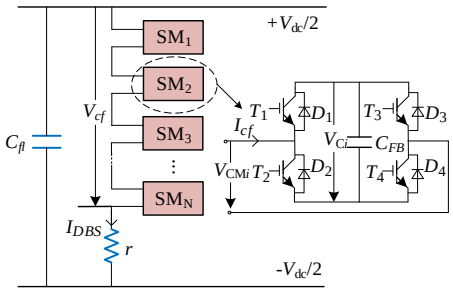


Fig.3. *The structure diagram of FB-DBS*

3.2. The operation principle of cascaded FBSM

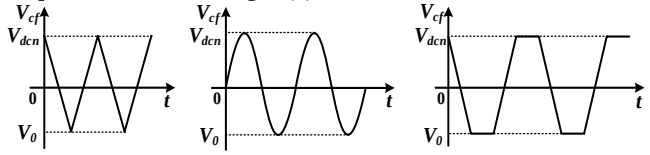
In normal operation, the sum output voltage of cascaded FBSM (V_{cf}) is controlled equally to the rated DC voltage (V_{dcn}) to ensure the system power is not absorbed by FB-DBS.

When DC faults happen, the fault line is firstly isolated by DCCBs within 3ms. With the feeding power of wind farm plants, the discharge of WFMMC is not obvious. Then, the DC current and power can be forced into the FB-DBS by

reducing V_{cf}. As V_{cf} is determined by states of the fully controlled IGBTs, the power dissipated on r can be controlled by proper operation strategies of the cascaded FBSM. Due to the unidirectional DC current, to avoid continually charging of FBSMs, V_{cf} should maintain a negative value for a period. Under a reasonable control strategy, each of the FBSMs can maintain energy balance during a control cycle T. Considering the voltage balance among the sub-modules during the fault, the control cycle T generally adopts a medium frequency (MF) cycle signal (300~500Hz) to meet the requirements of frequent insertion of FBSMs.

When AC faults happen at grid side, DCCBs maintain closed and the unbalanced power causes rise of DC voltage. It will further cause the overvoltage of sub-module capacitors. In this period, FB-DBS is utilized to absorb the unbalanced power to protect MMCs. Its output voltage control principle during AC faults is the same as that during DC faults.

According to the above analysis, several feasible modulation strategies to generate the reference voltage of the cascaded FBSM in this paper are shown in Fig.4. To simplify the calculation and equation derivation, the symmetrical isosceles trapezoidal wave modulation is adopted as shown in Fig.4 (c).



(a) triangle wave *(b) sine wave* *(c)trapezoidal wave*

Fig.4. *Available modulation waves for the cascaded FBSM*

The output voltage of the cascaded FBSM changes periodically between V_{dcn} and V_0. To describe the internal and external characteristics of the cascaded FBSM in different stages, its output voltage, instantaneous power and energy in period T are shown in Fig.5.

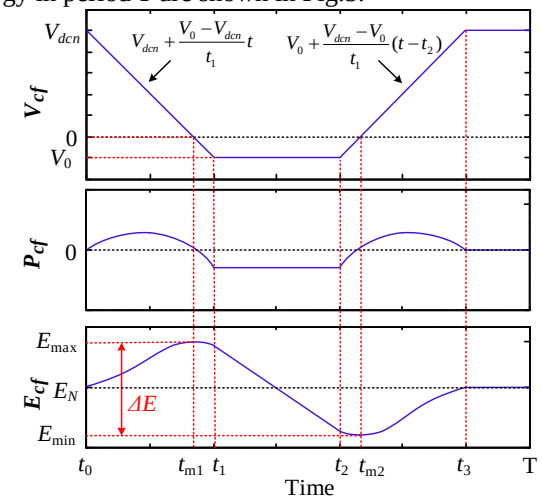


Fig.5. *The voltage, power and energy of the cascaded FBSM in a period T*

According to the voltage change of V_{cf}, one cycle can be divided into four stages. At the beginning of the first period [t_0, t_1], V_{cf}=V_{dcn} and then V_{cf} is linearly decreased to V_0, forcing DC current to flow through the FB-DBS branch, where V_0 is a negative value to ensure that the energy absorbed by the cascaded FBSM during [t_0, t_1] can be released by negatively inputting FBSMs in the next stage. In the next stage [t_1, t_2], the cascaded FBSMs generate V_0 to release energy into the dissipation resistor r so that the E_{cf} can be controlled zero in one cycle. Then, V_{cf} ascends to V_{dcn} in stage [t_2, t_3], where t_3 is the end time of voltage control in one cycle. Thus, the working state of FB-DBS can be changed by controlling t_3. When the system is in normal operation, t_3=0; when the system is under faults, t_3 is rapidly increased to T. Besides, t_{m1} and t_{m2} are the instantaneous moment where the voltage of cascaded FBSMs crosses 0, corresponding to the maximum and minimum energy moments of the cascaded FBSM respectively.

From the above analysis, the voltage of the cascaded FBSMs can be derived

$$V_{cf}=\begin{cases} V_{dcn}+\dfrac{V_0-V_{dcn}}{t_1}t & (0\le t<t_1) \\ V_0 & (t_1\le t<t_2) \\ V_0+\dfrac{V_{dcn}-V_0}{t_1}(t-t_2) & (t_2\le t<t_3) \\ V_{dcn} & (t_3\le t<T) \end{cases} \tag{1}$$

Under ideal conditions, the DC terminal voltage of the WFMMC is the rated DC voltage. The DC current flowing through the DBS can be derived

$$I_{cf}=\begin{cases} \dfrac{V_{dcn}-V_0}{rt_1}t & (0\le t<t_1) \\ \dfrac{V_{dcn}-V_0}{r} & (t_1\le t<t_2) \\ \dfrac{V_{dcn}-V_0+\dfrac{V_0-V_{dcn}}{t_1}(t-t_2)}{r} & (t_2\le t<t_3) \\ 0 & (t_3\le t<T) \end{cases} \tag{2}$$

To maintain energy balance in the cascaded FBSMs, the energy storage should equal to zero in one cycle, which can be obtained

$$\begin{aligned} \sum E_{cf}=&\int_0^{t_1}(V_{dcn}+\frac{V_0-V_{dcn}}{t_1}t)(\frac{V_{dcn}-V_0}{rt_1}t)\mathrm{d}t+\int_{t_1}^{t_2}\frac{V_0(V_{dcn}-V_0)}{r}\mathrm{d}t \\ &+\int_{t_2}^{t_3}\left[V_0+\frac{V_{dcn}-V_0}{t_1}(t-t_2)\right]\left[\frac{V_{dcn}-V_0+\dfrac{V_0-V_{dcn}}{t_1}(t-t_2)}{r}\right]\mathrm{d}t=0 \end{aligned} \tag{3}$$

In the isosceles trapezoid modulation of arm voltage, it can be derived

$$t_2=t_3-t_1 \tag{4}$$

Substituting (4) into equation (3), it can be derived

$$t_1=\frac{3V_0t_3}{4V_0-V_{dcn}} \tag{5}$$

According to Fig.5, t_2>t_1. Substitute it into equation (5):

$$-\frac{1}{2}V_{dcn}<V_0<0 \tag{6}$$

In condition of V_{dcn}=640kV, the inner relationship between t_1, V_0 and t_3 is shown in Fig.6.

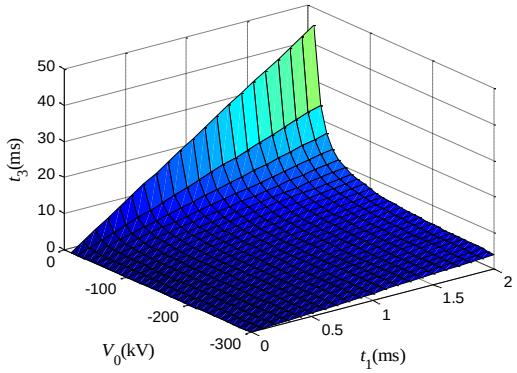


Fig.6. *The inner relationship between t_1, V_0 and t_3*

Defining duty cycle D_{cy} as t_3/T, the trapezoidal wave of the cascaded FBSM output voltage signal can be realized by the algorithm of Fig.7.

First, the specific moment of t_1, t_2, and t_3 are determined according to the four input signals D_{cy}, T, V_0, and V_{dcn}. If D_{cy}>0, calculate the output voltage of the cascaded FBSM according to the segmentation function(1). Otherwise, the output voltage directly outputs the rated DC voltage V_{dcn}.

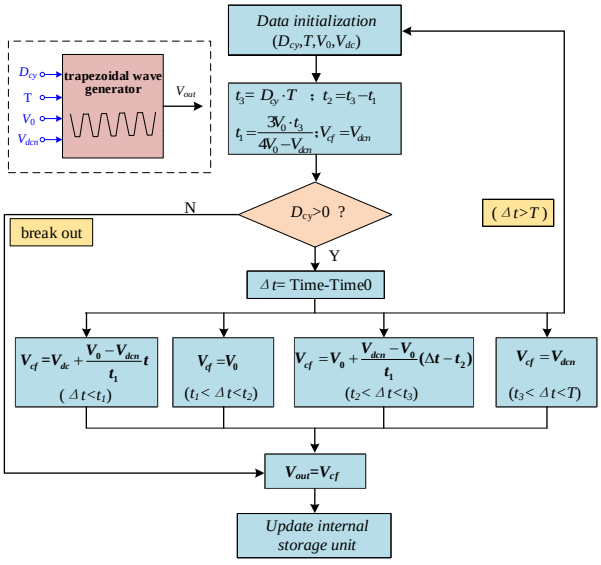


Fig.7. *Modulation algorithm of the trapezoidal wave generator*

3.3. The control strategy of FB-DBS

According to the procedure of aforementioned isosceles trapezoidal wave modulation, the operating state of FB-DBS depends on the D_{cy}. The model is based on the assumption that each sub-module capacitor voltage is well balanced by the voltage balancing algorithm. The discrete switching process is considered to be continuous. Thus, the DBS can be equivalent to RC series circuit. According to Kirchhoff's voltage law,

$$r\frac{C_{FB}}{N_{cf}}\frac{dV_{cf}}{dt}+V_{cf}=V_{dc} \tag{7}$$

Substituting equations (4)(5) and D_{cy}=t_3/T into (1) can obtain

$$V_{cf}=\begin{cases} V_{dcn}+\dfrac{(V_0-V_{dcn})(4V_0-V_{dcn})}{3V_0D_{cy}\mathrm{T}}t & (0\le t<t_1)\\ V_0 & (t_1\le t<t_2)\\ V_0+\dfrac{(V_0-V_{dcn})^2}{3V_0}+\dfrac{(V_{dcn}-V_0)(4V_0-V_{dcn})}{3V_0D_{cy}\mathrm{T}}t & (t_2\le t<t_3)\\ V_{dcn} & (t_3\le t<T) \end{cases} \tag{8}$$

Combining equations (7) and (8), it can be seen that V_{dc} is directly affected by D_{cy}. Thus, D_{cy} can be derived through the proportional-integral (PI) regulator by detecting the changes of V_{dc}.

$$D_{cy}=K_{i1}\int(V_{dcpu}-V_{dc\_lim})dt+K_{p1}(V_{dcpu}-V_{dc\_lim}) \tag{9}$$

In normal operation, the DC voltage is controlled around the rated value and the duty cycle generator finally outputs 0 after passing through the limiter. When the DC line voltage rises, V_{dcpu_DBS} will exceed the threshold V_{dc_lim}(1.05*pu*). The deviation is sent to a PI controller to generate D_{cy}, which is limited in the range of 0-1.

Under the trapezoidal modulation mode, FBSMs are periodically charged and discharged, so there is a deviation between each V_{ci} and the rated value V_{cn}, which affects the cascaded FBSM output voltage V_{cf}. According to the structure of cascaded FBSM, there is:

$$\frac{dV_{cf}}{dt}=\frac{d\sum V_{ci}}{dt} \tag{10}$$

Define the V_{c_avg} as the average capacitance voltage of the cascaded FBSMs, as shown below.

$$V_{c\_avg}=\frac{\sum V_{ci}}{N_{cf}V_{cn}} \tag{11}$$

where N_{cf} is the number of the cascaded FBSMs. Thus, combining equation(7), (10) and (11) can obtain

$$rC_{FB}V_{cn}\frac{dV_{c\_avg}}{dt}+V_{cf}=V_{dc} \tag{12}$$

When the trapezoidal wave generator starts to operate according to the signal D_{cy}, the system power is rebalanced. In a given operating state, the small signal equation can be obtained from (12):

$$rC_{FB}V_{cn}\frac{d\Delta V_{c\_avg}}{dt}+\Delta V_{cf}=0 \tag{13}$$

Thus, an average capacitor voltage control is utilized to suppress the deviation of the cascaded FBSM output voltage:

$$\Delta V_{cf}=K_{i2}\int(V_{c\_avg}-1)dt+K_{p2}(V_{c\_avg}-1) \tag{14}$$

In Fig.8, the deviation between 1 and V_{c_avg} is fed into a PI controller to generate the offset voltage. By adding a negative compensation at V_{cf_ref} (under the situation that cell capacitor voltages are higher than reference), the number of negatively inserting SMs can be increased, which will make the cell capacitor voltages reduce, and vice versa. The final reference voltage of full-bridge arm, V_{demand_ref}, uses nearest level modulation (NLM) and cell capacitor voltage balancing control to generate switching pulse and the arm outputs the desired V_{arm}.

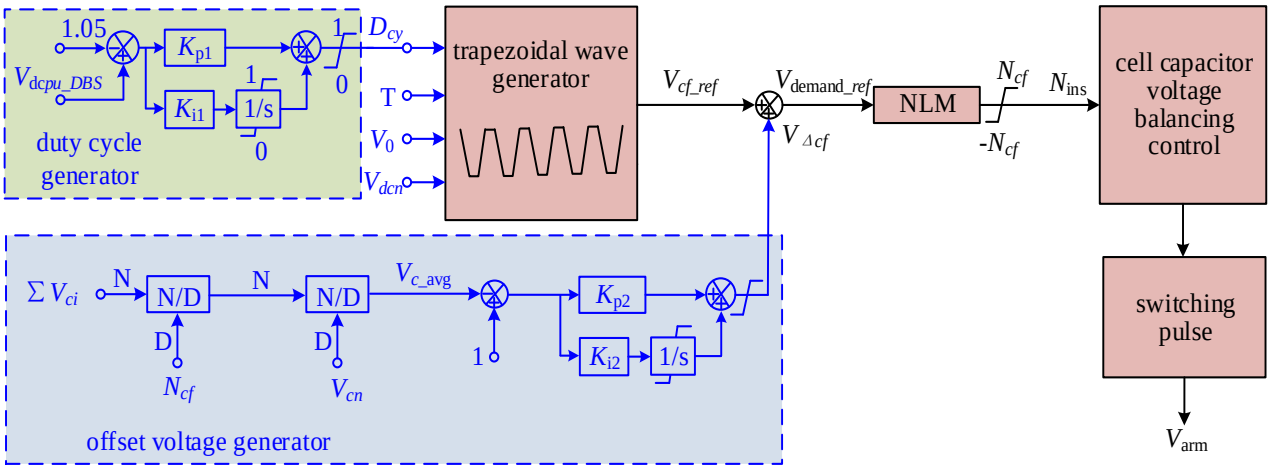


Fig.8. *The control strategy of FB-DBS.*

3.4. The parameter design of the FB-DBS

As for the parameter design of the FB-DBS, the number of cascaded sub-modules N_{cf}, the cell capacitance C_{FB} and the energy dissipation resistance r are important factors. These values determine the cost, cell voltage ripple and allowable current and voltage of FB-DBS.

N_{cf} is determined by the rated DC voltage of HVDC system V_{dcn} and the rated voltage of semiconductors V_{cn} in the FBSM. It can be calculated as:

$$N_{cf} = V_{dcn} / V_{cn} \tag{15}$$

As C_{FB} directly affects the capacitor voltage fluctuation and construction cost of FB-DBS, it is essential to select the proper capacitance. The SM capacitance voltage ripple can be derived from the maximum energy fluctuation of the cascaded FBSM, which is corresponding to the ΔE in Fig.5.

The maximum and minimum energy of the cascaded FBSM are

$$\begin{cases} E_{\max} = \int_0^{t_{m1}} (V_{dcn} + \frac{V_0 - V_{dcn}}{t_1} t) \cdot (\frac{V_{dcn} - V_0}{r t_1} t) dt \\ E_{\min} = \int_{t_{m2}}^{t_3} [V_0 + \frac{V_{dcn} - V_0}{t_1} (t - t_2)][\frac{V_{dcn} - V_0 + \frac{V_0 - V_{dcn}}{t_1}(t - t_2)}{r}] dt \end{cases} \tag{16}$$

where

$$\begin{cases} t_{m1} = \dfrac{V_{dcn} \cdot t_1}{V_{dcn} - V_0} \\ t_{m2} = t_3 - t_{m1} \end{cases} \tag{17}$$

The maximum energy fluctuation of FBSM can be then calculated as:

$$\Delta E_c = \frac{1}{2} C_{FB} [V_c^2 (1+\varepsilon)^2 - V_c^2 (1-\varepsilon)^2] \tag{18}$$

Thanks to the sub-module sorting and voltage equalization algorithm, the capacitance voltage fluctuation of each FBSM is considered to be approximately the same, and the relationship between the capacitor voltage and the energy of the cascaded FBSM is obtained as:

$$\Delta E_c = \frac{E_{\max} - E_{\min}}{N_{cf}} \tag{19}$$

Considering the most serious case where the duty cycle D_{cy}=1, substitute equation (5), (16)-(18) into equation (19):

$$C_{FB} \approx \frac{2 V_{dcn}^3 \cdot V_0 \cdot T}{(4V_0 - V_{dcn}) \varepsilon r V_c^2 N_{cf} (V_{dcn} - V_0)} \tag{20}$$

In equation(20), all parameters have been obtained except ε and r. The design of r is analyzed below.

According to (1) and(2), the voltage, power and energy of r in a period T can be depicted as shown in Fig.9. Voltage drop on r can be described as $V_r = V_{dcn} - V_{cf}$, which rises from zero to $V_{dcn} - V_0$ in [0, t_1]. In [t_1, t_2], V_r maintains V_{dcn}-V_0. From t_2, V_r descends to zero and r completes the power dissipation process at t_3.

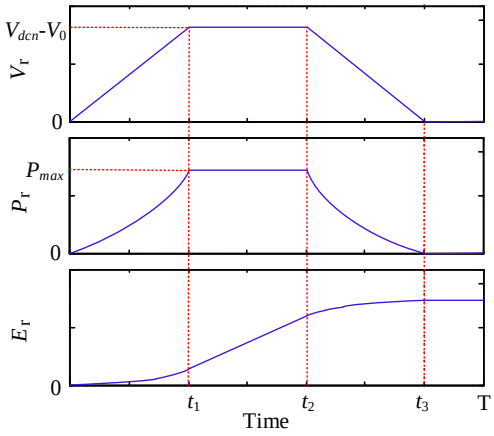


Fig.9. *The voltage, power and energy of dissipation resistor r in a period T*

When D_{cy}=0, V_{cf} always equals V_{dc} and V_r equals zero, i.e. there is no power dissipated on r; When D_{cy}=1, all the wind power is consumed by r; When 0<D_{cy}<1, FB-DBS dissipates part of wind power. The energy absorbed by r is calculated as:

$$\sum E_r = 2 \int_0^{t_1} (\frac{V_{dcn} - V_0}{t_1})^2 \frac{t^2}{r} dt + \frac{(V_{dcn} - V_0)^2}{r} (t_3 - 2t_1) \tag{21}$$

And equation (22) can be obtained by substituting equation (5) into equation (21):

$$\sum E_r = \frac{(V_{dcn} - V_0)^2}{r} \cdot \frac{V_{dcn}}{V_{dcn} - 4V_0} t_3 \tag{22}$$

Therefore, the absorbing power of r can be depicted as

$$P_r = \frac{(V_{dcn} - V_0)^2}{r} \cdot \frac{V_{dcn}}{V_{dcn} - 4V_0} \tag{23}$$

The value of r can be designed as:

$$r = \frac{V_{dcn}(V_{dcn} - V_0)^2}{P_{dcn}(V_{dcn} - 4V_0)} \tag{24}$$

where P_{dcn} is the rated DC power.

Substituting equation (24) into equation (20) and considering the constraint of sub-module capacitor voltage ripple ε, the appropriate sub-module capacitance value can be obtained.

Due to the large harmonics of the wind farm and MMC feeding current to the FB-DBS during DC fault, the DBS needs to install a DC filter C_{fl} to avoid harmonic disturbance and the potential controller disorder. The stored energy in C_{fl} during a charge and discharge cycle is:

$$0.5C_{fl}(V_{\max}^2 - V_{\min}^2) = P_{dcn} \cdot T \tag{25}$$

Simplifying equation (25), C_{fl} is determined as:

$$C_{fl} = \frac{P_{dcn} \cdot T}{2\varepsilon V_{dcn}^2} \tag{26}$$

In summary, once the parameters T, P_{dc}, V_{dc}, V_{ci}, V_0 and ε are known, all components of the FB-DBS can be determined. The FB-DBS can automatically dissipate transient wind energy during AC and DC faults, and its operation does not depend on the communication system as only local detection signals are needed. Moreover, the smoothly controlled *di/dt* and *dv/dt* bring a lower EMI to surroundings.

4. Control of Hybrid DCCB and The System FRT Strategy

4.1. Control of hybrid DCCB

Equivalent modeling of the hybrid DCCB depicted in Fig.2 is shown in Fig.10. The main branch is implemented by a fast mechanical dis-connector S_1 with a 2ms break delay and a LCS. It allows residual current I_{res} with a typical value of 0.01kA. The commutation branch is equivalent by IGBTs and anti-parallel diodes. The absorption branch adopts the MOV model provided by PSCAD.

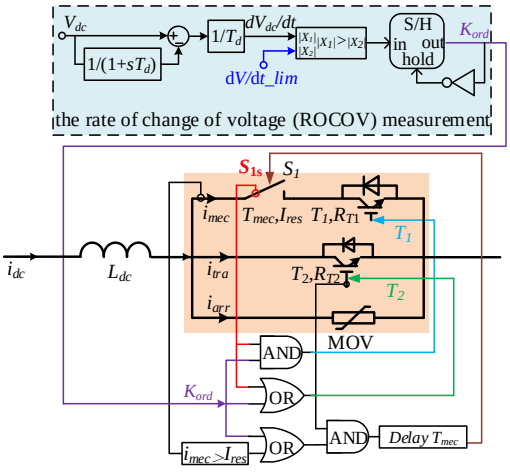


Fig.10. *Control logic of hybrid DCCB*

Denote K_{ord} as the upper level command signal sent into DCCB. K_{ord}=1 represents that the DCCB is turned on, while K_{ord}=0 indicates that the DCCB is turned off. To detect DC faults, a travelling wave measuring method based on line side DC voltage change rate [21] is used in this paper, as the dashed frame shows in Fig.10. When dV_{dc}/dt is large than the setting threshold *dV/dt_lim*, the system judges an occurrence of DC fault and DCCB can be tripped immediately.

In the normal operation (K_{ord}=1), S_1 is closed after T_{mec} (with a typical value of 2ms) delay and then T_1 and T_2 are conductive. Since the on-state resistance of T_1 branch is far lower than T_2 branch, almost entire i_{dc} passes through T_1 path, which guarantees the low loss of DCCB.

When K_{ord}=0, T_1 is firstly turned off, then i_{mec} starts to decrease while i_{tra} increases. As i_{mec} drops below I_{res}, S_1 is completely opened after 2ms delay. Then T_2 is turned off and the current is forced to flow into the MOV arrester branch. At last, i_{arr} decreases to zero and DCCB accomplishes opening procedure. When K_{ord}=1, T_2 is firstly turned on. Then S_1 and T_1 are closed successively. According to the analysis above, the control logic can be describe as shown in equations (27)-(29):

$$T_1 = K_{ord} \text{ AND } S_{1s} \tag{27}$$

$$T_2 = K_{ord} \text{ OR } S_{1s} \tag{28}$$

$$S_1 = \left(K_{ord} \text{ OR } \left(i_{mec} > I_{res}\right)\right) \text{ AND } T_2 \tag{29}$$

where S_{1S} denotes the state of S_1.

4.2. AC and DC FRT strategies of the wind power integration system

When AC faults happen at grid side, the DC fault current is lower than the rated value and the DC voltage rise caused by unbalanced power will not trigger DCCBs, so that DCCBs will not trip. If DC faults happen, the DCCBs should be quickly tripped to isolate the fault line and then FB-DBS activates to absorb surplus wind power. During the opening state of DCCBs, the WFMMC remains operating and supporting the AC voltage of the PCC. Overall, the AC and DC faults ride-through strategies of the wind power integration system are shown in Fig.11.

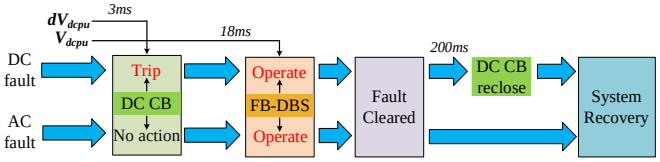


Fig.11. *AC and DC FRT strategies of the wind power integration system*

Assuming an AC fault occurs at the valve side of GSMMC, as the wind power is continuously transmitted to HVDC link, the unbalanced power of GSMMC brings about rise of DC voltage. When the DC voltage exceeds the threshold of 1.05pu, FB-DBS switches on to absorb the wind power. The dissipation resistor r should be able to tolerate the maximum voltage during faults. Considering that the overvoltage of HVDC line is in the range of 1.2pu, the maximum withstands voltage of r should be no less than,

$$V_{rmax} = 1.2 \cdot V_{dcn} - V_0 \tag{30}$$

After the fault is eliminated, FB-DBS gradually reduces its absorbing power and then the system recovers power transmission.

In case of a DC fault, DCCBs will be immediately tripped (within 3ms) as the dV_{dc}/dt exceeds the setting threshold modulus *dV/dt_lim*, and then the power transmission only exists between wind power plants and WFMMC. Once the FB-DBS switches on, most of the wind energy is absorbed by FB-DBS. Assuming the DC fault is non-permanent, after

the fault current is isolated, DCCBs will reclose after deionization time, typically 200ms, and the system recovers to normal operation quickly.

5. Simulation Verification

5.1. Parameters of the simulated system

The system of

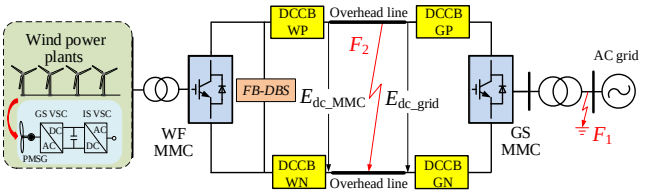


Fig.*1* is built on PSCAD/EMTDC. According to equations (20), (24) and (26), parameters of the simulated system including C_{FB}, C_{fl}, and r are listed in Tab.1. The constants and thresholds in the system are shown in Tab.2.

Tab.1. System parameters

parameters	value
MMC rated power (MVA)	1000
Rated wind power (MVA)	1000
Rated DC voltage (kV)	±320
AC output voltage of wind farm (kV)	230
The length of overhead line (km)	300
DC reactor L_{dc} (mH)	130
SM capacitance of MMC (μF)	4888
Number of SMs per arm of MMC	200
Number of FB SMs in DBS	160
SM capacitance of FB-DBS (μF)	4000
Lumped capacitance of FB-DBS (μF)	50
The dissipation resistor r (Ω)	327
FBSM capacitor voltage ripple ε	0.05

Tab.2. Constants and thresholds of the system

parameters	value	parameters	value
I_{am}(kA)	2.315	dV/dt_lim	500
I_{pam}(kA)	1.67	V_0(kV)	-128
V_{rmax}(pu)	1.4	T(s)	0.002

5.2. System response to AC fault

A temporary three-phase AC fault lasting 0.1s is applied at F_1 at 1.2s, as shown in

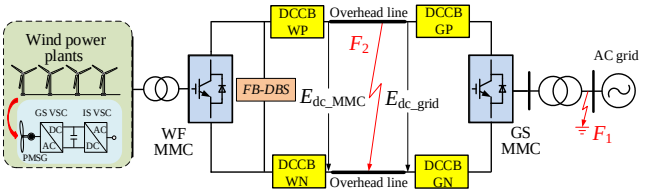
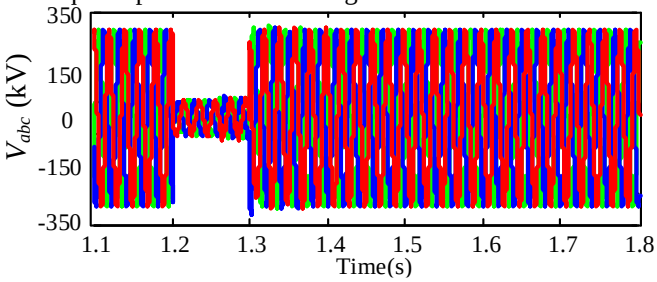
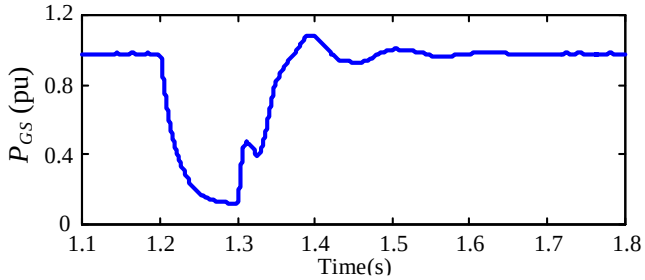


Fig.*1* of GSMMC. Fig.12 and Fig.13 show the system response to AC fault.

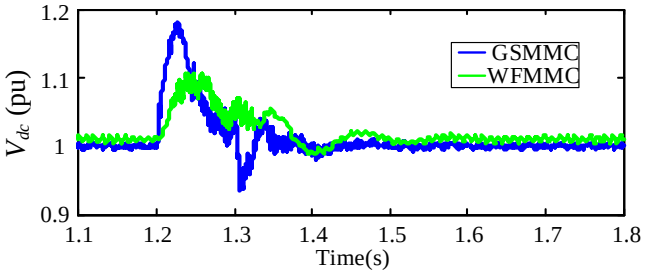
Fig.12 (a)-(d) respectively shows the AC side voltage of GSMMC, DC voltage at GSMMC, DC voltage at WFMMC, and DC power of GSMMC. Fig.12 (a) shows that AC side voltage of GSMMC will decrease to 0.1pu at 1.2s (due to the 0.01Ω fault transition resistance) and will restore to 1.0pu at 1.3s. The DC power delivered to the grid side from GSMMC reduces because of the AC fault, as shown in Fig.12 (b). The unbalanced power causes the rise of DC voltage at WFMMC and GSMMC, as shown in Fig.12(c). Due to existence for DC reactors and overhead lines, there is a DC voltage gap between GSMMC and WFMMC. Fig.12 (d) shows the AC voltage of the integration point is controlled to be stable. When the DC voltage at DBS exceeds 1.05pu, DBS is automatically activated to dissipate the surplus wind power to limit the rise of DC voltage. DC voltage and DC power are restored to pre-fault value and DBS quits operation after distinguish of AC fault.



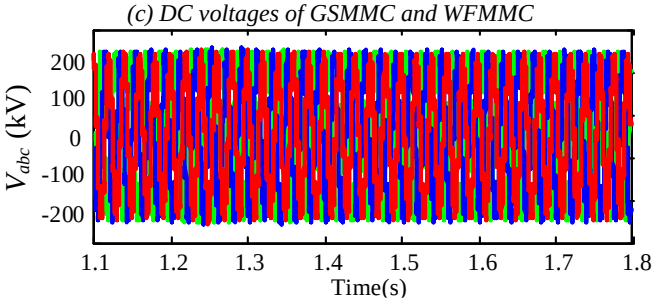
(a) AC voltage of GSMMC



(b) DC power delivered to the grid side from GSMMC



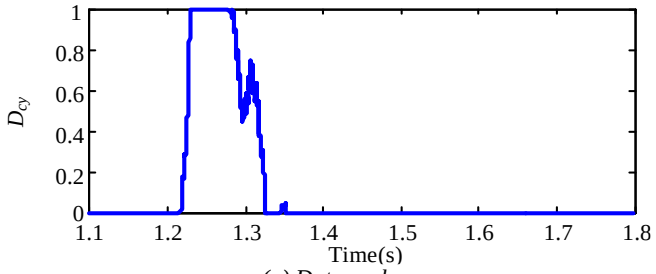
(c) DC voltages of GSMMC and WFMMC



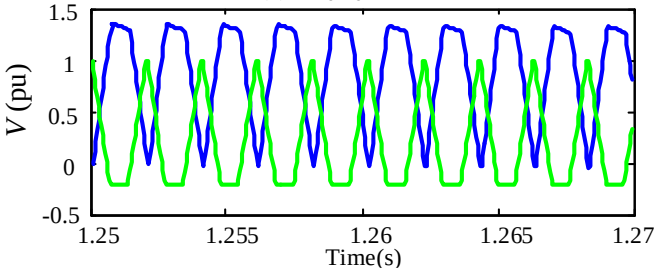
(d) AC voltage of WFMMC

Fig.12. *Simulation waveforms of GSMMC and WFMMC under the AC fault*

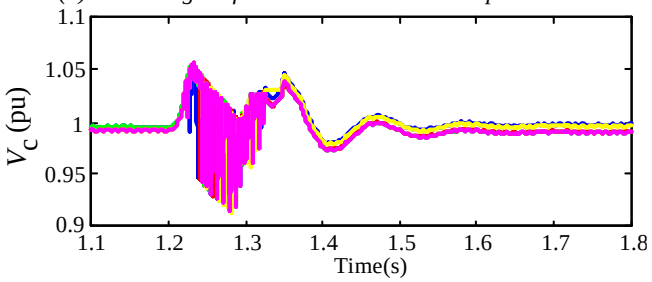
Fig.13(a)-(d) respectively shows the duty cycle, the voltages of the cascaded FBSM and the lumped resistor, SM voltages of the FBSMs and the power dissipated by the lumped resistor. Operation of the DBS is in accordance with the analysis of section 3. When the AC three-phase fault occurs, the duty cycle will increase to 1 after DC voltage exceeds 1.05pu, as shown in Fig.13 (a). The voltage of cascaded FBSMs and the voltage across dissipation resistor r are presented as trapezoidal in Fig.13 (b). Cell capacitor voltages can be balanced around the ripple of 5%, as shown in Fig.13 (c). During the fault, the surplus wind power can be totally absorbed by DBS as shown in Fig.13 (d). After the fault clearance, duty cycle and wind power absorbed by DBS decrease down to zero, and cell capacitor voltages go back to 1.0pu finally.



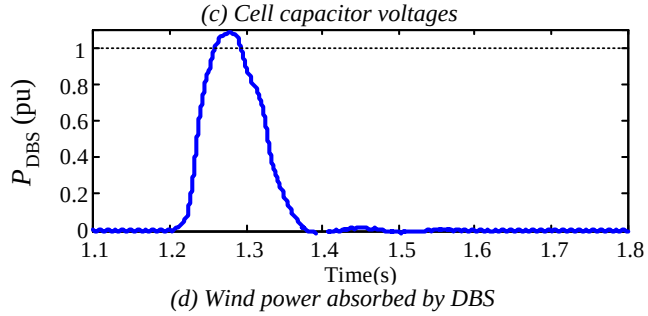
(a) Duty cycle



(b) The voltages of cascaded FBSM and lumped resistor



(c) Cell capacitor voltages



(d) Wind power absorbed by DBS

Fig.13. *Simulation waveforms of DBS under the AC fault*

5.3. System response to DC fault

In

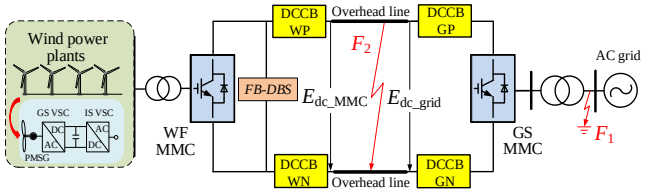
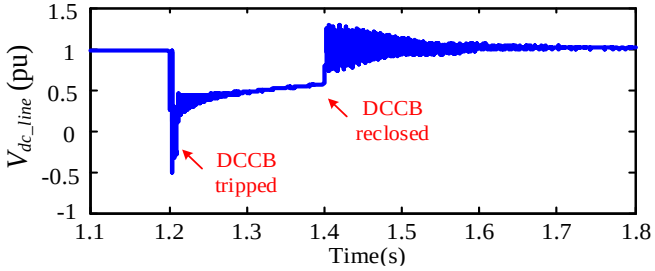
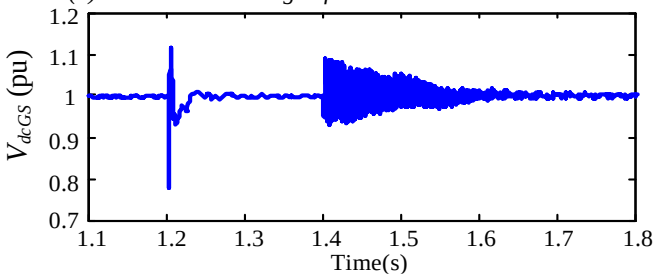


Fig.***1***, a pole-to-pole DC fault is set at F_2. The fault occurrence time is 1.2s, and its duration is 0.1s. DCCBs are tripped after detecting the DC fault and wait for 200ms to reclose.

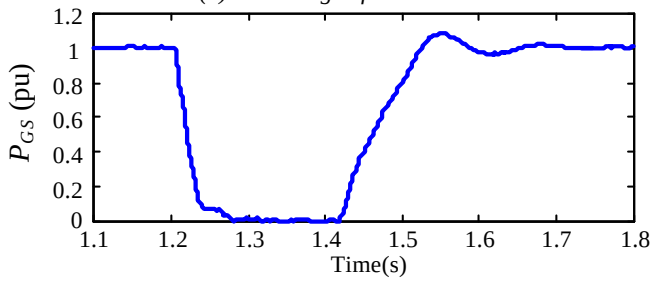
Fig.14 (a) shows that DC line voltage of DCCB GP and DCCB GN drops to zero and reverse polarity because of the overhead line flashover discharge. And then it oscillates at high frequency because the overhead line has a low value of capacitance to earth. Fig.14 (b) shows that the DC voltage of GSMMC drops to 0.78pu at 2.5ms after the fault occurred. When DCCBs have tripped, the rapid attenuation of DC current brings a spike in DC voltage. Then, the DC voltage can maintain 1.0pu after DCCBs break off completely and will restore to around 1.0pu at 1.8s after DCCBs reclose. Fig.14 (c) shows the active power of GSMMC decreases to zero after turning off of DCCBs. Fig.14 (d) shows the peak value of DC current of the overhead line is 2.6pu. The DC current decreases to zero after DCCBs are tripped and recovers to rated value after reclosure of DCCBs.



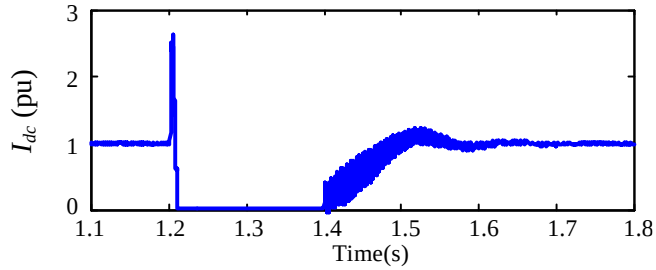
(a) Line side DC voltage of DCCB GP and DCCB GN



(b) DC voltage of GSMMC



(c) Active power delivered to the grid side from GSMMC



(d) DC current of the overhead line

Fig.14. *Simulation waveforms of the GSMMC and HVDC link under the DC fault*

Fig.15 shows the response of WFMMC during pole-to-pole DC fault and reclosing period. Fig.15 (a) shows that the DC voltage of WFMMC firstly reduces to 0.87pu and after isolation of DC fault current, it rises to 1.2pu because of the surplus wind power from PMSG wind power plants. Meanwhile, DBS is put into operation to dissipate wind power and then the DC voltage declines and fluctuates around 1.05pu. After reclosing at 1.4s, it recovers to normal value gradually. Fig.15 (b) shows that arm current increases to 1.58pu of rated peak value because of the increase DC component. The peak value of arm current remains within

twice times of the rated value, which guarantees the uninterrupted operation of WFMMC. Fig.15 (c) shows the received wind power of WFMMC. Fig.15 (d) shows that the AC current of phase *A* stays unchanged because WFMMC still can control its AC side current at an unblocking status.

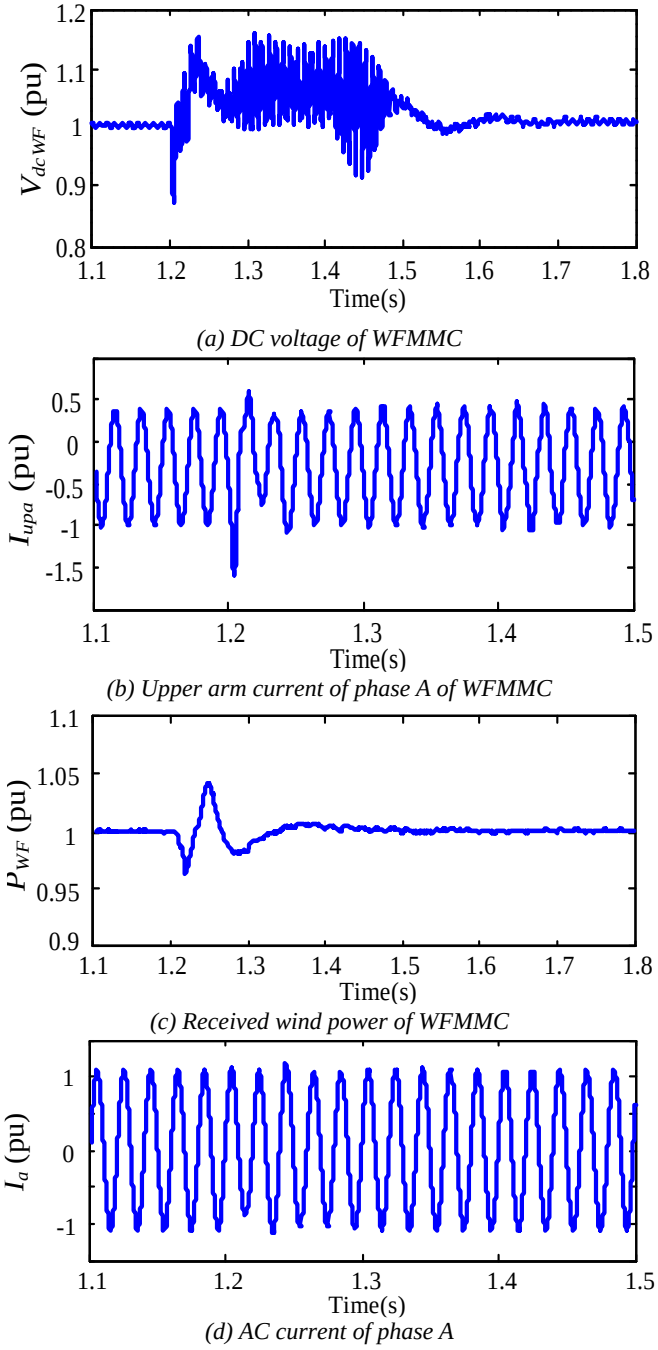


Fig.15. *Simulation waveforms of WFMMC under the DC fault*

Fig.16 shows the response of DBS and DCCB during DC fault at F_2. Fig.16 (a) shows that the duty cycle increases after DCCBs are tripped and DBS begins to absorb the surplus wind power. Voltage of the cascaded FBSMs and voltage across the dissipation resistor are both trapezoidal as shown in Fig.16 (b). Cell capacitor voltages are controlled around the ripple of 5% as shown in Fig.16 (c). After reclosure of DCCBs, the duty cycle decreased to zero, and cell capacitor voltages recover to 1.0pu gradually. The energy absorbed by MOV in Fig.16 (d) is no more than 7.1MJ.

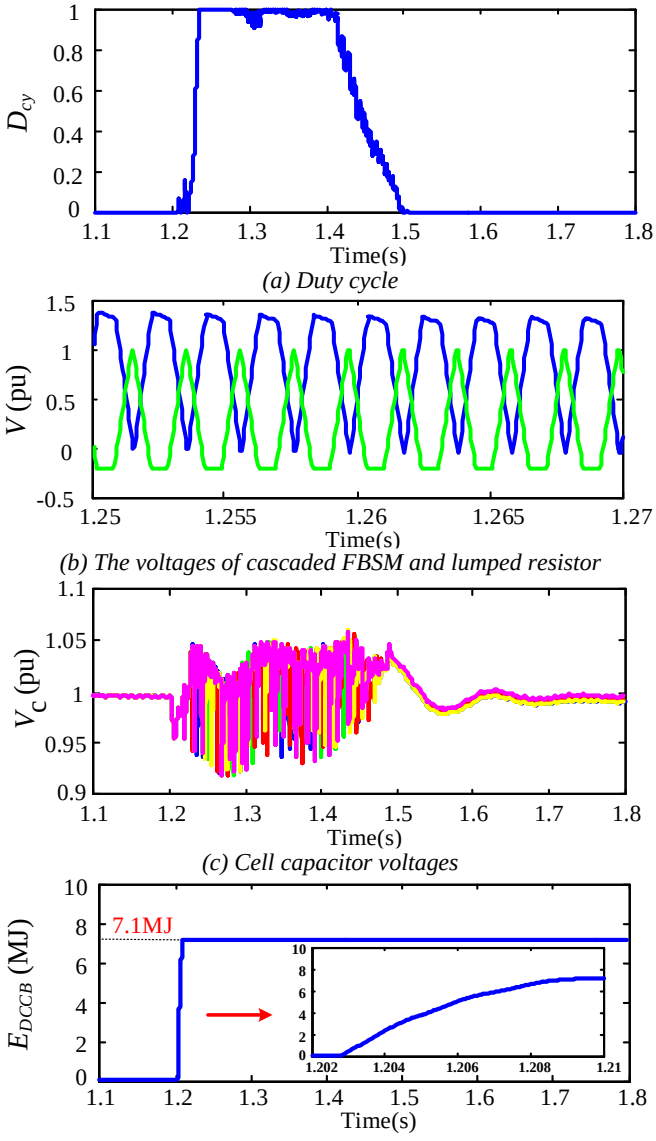


Fig.16. *Simulation waveforms of DBS and DCCB under the DC fault*

6. Conclusion

In this paper, an energy dissipation device, FB-DBS, is designed to absorb the surplus wind power during AC and DC fault in MMC-HVDC wind power integration system. Based on the analysis of the operating principle of FB-DBS, comprehensive control strategies and parameter design of the FB-DBS are proposed. The FB-DBS can operate without communication system for only local detection signals are in need, and the smoothly controlled *di/dt* and *dv/dt* bring a lower EMI to surroundings. A travelling wave method based on measuring the rate of change of line side DC voltage is adopted to trip hybrid DCCBs to interrupt DC fault current rapidly and correctly. Besides, the control of hybrid DCCB and the system FRT strategies during AC and DC faults are proposed. The simulation shows that FB-DBS can suppress the peak arm current within 1.5pu under the DC fault and

maintain the DC link voltage in the range of 1.2pu under AC fault.

7. Acknowledgments

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8. References

[1] A. Perez, S. Bernet, J. Rodriguez, et al.: 'Circuit topologies, modeling, control schemes, and applications of modular multilevel converters', IEEE Transactions on Power Electronics, 2015, 30, (1), pp. 4-17.

[2] J. C. Qin, M. Saeedifard, A. Rockhill, et al.: 'Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits', IEEE Transactions on Power Delivery, 2015, 30, (1), pp. 385-394.

[3] J. Lyu, X. Cai, M. Molinas.: 'Frequency Domain Stability Analysis of MMC-Based HVDC for Wind Farm Integration', IEEE Journal of Emerging and Selected Topics in Power Electronics, 2016, 4, (1), pp. 141-151.

[4] 'GWEC Global Wind Report 2018', http://www.gwec.net/, accessed April 2019.

[5] R. Vidal, H. Beltran, A. Rolan, et al.: 'Analysis of the Performance of MMC under Fault Conditions in HVDC-based Off-shore Wind Farms', IEEE Transactions on Power Delivery, 2016, 31, (2), pp. 1-9.

[6] Yousef pipelzadeh, Nilanjan ray chaudhuri, Balarko chaudhuri, et al.: 'Coordinated Control of Offshore Wind Farm and Onshore HVDC Converter for Effective Power Oscillation Damping', IEEE Transactions on Power Systems, 2017, 32, (3), pp. 1860-1872.

[7] 'Van Oord–Hellenic Cables consortium assigned to connect Hollandse Kust (South) project to grid', https://iro.nl/news-and-press/van-oord-hellenic-cables-consortium-assigned-to-connect-hollandse-kust-south-project-to-grid/, accessed 7 September 2018.

[8] 'ABB wins offshore wind connection project in German North Sea',https://new.abb.com/news/detail/13326/abb-wins-offshore-wind-connection-project-in-german-north-sea/, accessed 21 October 2013.

[9] 'Peikko Group delivers rock foundation technology for Norwegian wind farm', https://www.renewableenergymagazine.com/wind/peikko-group-delivers-rock-foundation-technology-for-20170815, accessed 15 August 2017.

[10] Neha Korde, Narendra Bhagat.: 'A novel fault monitoring mechanism on overhead transmission line in power grid', 2017 International Conference on Intelligent Computing and Control (I2C2), Jun. 2017. DOI: 10.1109/I2C2.2017.8321832.

[11] Xiaojie Shi, Yalong Li, Leon M. Tolbert, Fred Wang.: 'Cascaded droop control for dc overvoltage suppression in a multi-terminal HVDC system under onshore side AC faults', 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), May. 2016. DOI: 10.1109/IPEMC.2016.7512876.

[12] B. silva, C. l. moreira, H. leite, et al.: 'Control Strategies for AC Fault Ride Through in Multiterminal HVDC Grids', IEEE Transactions on Power Delivery, 2014, 29, (1), pp. 395-405.

[13] G. Tarnowski, P. C. Kjaer, R. Laerke, F. Iov, R. Teodorescu, and A. Adamczyk.: 'Power plant and energy storage system for provision of grid ancillary services', WIPO Patent PCT/DK2013/050 032, accessed 7 February 2013.

[14] Ahmed moawwad, Mohamed shawky el moursi, Weidong Xiao.: 'Advanced Fault Ride-Through Management Scheme for VSC-HVDC Connecting Offshore Wind Farms', IEEE Transactions on Power System, 2016, 31, (6), pp. 4923-4934.

[15] C. C. Davidson, R. A. Mukhedkar.: 'A comparison of different types of Dynamic Braking System for HVDC systems for offshore wind power', Proc. of Cigr é Brussels, Brussels, Belgium, Mar. 2014, pp. 1-8.

[16] S. Cao, W. Xiang, L. Z. Yao, et al.: 'AC and DC fault ride through hybrid MMC integrating wind power', The Journal of Engineering, 2017, (13), pp. 828-833.

[17] A. Hassanpoor, J. Hafner, and B. Jacobson.: 'Technical assessment of load commutation switch in hybrid hvdc breaker', IEEE Transactions on Power Electronics, 2015, 30, (10), pp. 5393-5400.

[18] N. Christoph, H. Jen, H. Robert, and V. H. Dirk.: 'Application of DC Choppers in HVDC Grids', 2016 IEEE International Energy Conference (ENERGYCON), Jul. 2016. DOI: 10.1109/ENERGYCON.2016.7513951.

[19] J. Maneiro, S. Tennakoon, C. Barker, et al.: 'Energy diverting converter topologies for hvdc transmission systems', 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, Oct. 2013, pp. 1-10.

[20] W. Lin, D. Jovcic, S. Nguefeu, H. Saad.: 'Modelling of high-power hybrid DC circuit breaker for grid-level studies', IET Power Electronics, 2016, 9, (2), pp. 237-246.

[21] J. Sneath, A. D. Rajapakse.: 'Fault detection and interruption in an earthed hvdc grid using rocov and hybrid dc breakers', IEEE Transactions on Power Delivery, 2016, 31, (3), pp. 973-981.